LISTING OF THE CLAIMS

1. (Previously presented) A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer, wherein said bottom conducting layer is a bottom electrode;

an annealed dielectric layer formed over said bottom conducting layer, wherein said annealed dielectric layer is annealed with a first annealing process; and

a top electrode consisting of a single oxidized gas annealed top conducting layer formed over said annealed dielectric layer, wherein said annealed top conducting layer is annealed with a second annealing process.

2. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

3. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal.

4. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal alloy.

5. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a conducting metal oxide.

6. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal nitride.

7. (Original) The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2). Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN, or W2N).

8. (Original) The capacitor of claim 7, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN, or W_2N).

9. (Original) The capacitor of claim 1, wherein said bottom conducting layer is placed on top of an oxygen barrier.

10. (Original) The capacitor of claim 1, wherein said dielectric layer is a dielectric metal oxide layer.

11. (Original) The capacitor of claim 1, wherein said dielectric layer has a dielectric constant between 7 and 300.

12. (Original) The capacitor of claim 1, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (BST), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate.

13. (Original) The capacitor of claim 12, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

14. (Original) The capacitor of claim 13, wherein said dielectric layer is Tantalum Oxide and is amorphous or crystalline.

15. (Original) The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the noble metal group.

16. (Original) The capacitor of claim 1, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

17. (Original) The capacitor of claim 1, wherein said top conducting layer is formed of a conducting metal oxide.

18. (Original) The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from die group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

19. (Original) The capacitor of claim 18, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

20. (Original) The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

21. (Previously presented) The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said dielectric layer is a layer of Barium Strontium Titanate (BST).

22. (Previously Presented) The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN, or W_2N) layer and, said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

23. (Original) The capacitor of claim 1, wherein said top conducting layer is annealed with an oxygen compound.

24. (Original) The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

25. (Original) The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

26. (Previously presented) The capacitor of claim 23, wherein said annealed top conducting layer is a plasma enhanced annealed top conducting layer.

27. (Previously presented) The capacitor of claim 23, wherein said annealed top conducting layer is a remote plasma enhanced annealed top conducting layer.

28. (Previously presented) The capacitor of claim 23, wherein said annealed top conducting layer is an ultraviolet light enhanced annealed top conducting layer.

29. (Original) The capacitor of claim 1, wherein said capacitor is a stacked capacitor.

30. (Original) The capacitor of claim 1, wherein further comprising an access transistor connected to said capacitor.

31. (Original) The capacitor of claim 1, wherein said capacitor forms part of a dynamic random access memory cell.

Claims 32-98 (Canceled).

99. (Previously presented) A capacitor for a semiconductor device, said capacitor comprising:

a bottom electrode;

an annealed dielectric layer formed over said bottom electrode that has been annealed with a first oxidizing gas anneal process; and

an upper electrode comprising a top conducting layer which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process.